AMENDMENTS TO THE CLAIMS

Claims 1-12 (Cancelled)

13. (Previously Presented) An inductive amplifier, comprising:

a first stage coupled to receive an input signal and adapted to draw an output current from intermediate output nodes in response to the input signal, the first stage including

a first differential transistor pair having common first conductors coupled to a first node and having second and third conductors coupled to the intermediate output nodes; and

a first current source coupled to the first node and adapted to conduct the output current drawn from the first and second intermediate output nodes; and

a boost stage coupled to the intermediate output nodes and coupled to receive the input signal, the boost stage including

a second differential transistor pair having common first conductors coupled to a second node and having second and third conductors coupled to the intermediate output nodes; and

a second current source coupled to the second node and adapted to conduct the variable current drawn from the intermediate output nodes, wherein the boost stage is adapted to draw a variable current from the intermediate output nodes in response to a frequency of the input signal to modify a magnitude of the output current drawn.

Claims 14-15 (Cancelled)

16. (Previously Presented) The inductive amplifier of Claim 13, wherein a magnitude of the variable current drawn by the boost stage decreases with an increasing frequency of the input signal.

17. (Currently Amended) A method of boosting gain, comprising:

establishing a first current signal by dividing the first current signal into second and third current signals having respective magnitudes;

generating an output signal in response to an input signal, wherein a magnitude of the output signal is proportional to the magnitude of the third current signal; and

decreasing the magnitude of the [[first]] second current signal in response to an increasing frequency of the input signal, and as a result, increasing the magnitude of the third current signal to increase the magnitude of the output signal.

18. (Previously Presented) The method of claim 17, wherein generating the output signal comprises generating a voltage signal that is proportional to a difference between the first current signal and the second current signal.

19. (Previously Presented) An amplifier, comprising:

a first transistor coupled to receive a first input signal at a first node and adapted to provide a first output signal at a second node in response to the first input signal;

a first current source coupled to the first transistor at a third node and adapted to conduct a first current signal through the first transistor, wherein a magnitude of the first output signal is directly proportional to a magnitude of the first current signal;

a second transistor coupled to the second node and adapted to conduct a second current signal from the second node in response to the first input signal, wherein a sum of a magnitude of the second current signal and the magnitude of the first current signal is derived from the second node to be substantially equal to a magnitude of a master current signal; and

a second current source coupled to the second transistor at a fourth node to conduct the second current signal, wherein in response to an increasing frequency of the first input signal, the magnitude of the second current signal decreases and the magnitude of the first current signal increases.

20. (Previously Presented) The amplifier of Claim 19, further comprising a third transistor coupled to the third node and coupled to receive a second input signal

and adapted to conduct the first current signal in response to the second input signal to produce a second output signal, wherein a magnitude of the second output signal is directly proportional to the magnitude of the first current signal.

21. (Previously Presented) The amplifier of Claim 20, further comprising a fourth transistor coupled to the fourth node and coupled to receive the second input signal and adapted to conduct the second current signal in response to the second input signal, wherein in response to an increasing frequency of the second input signal, the magnitude of the second current signal decreases and the magnitude of the first current signal increases.

22. (New) An amplifier, comprising:

a boost circuit including,

a first transistor coupled to a first node and adapted to conduct a first current from the first node in response to a first phase of an input signal; and

a inductive amplifier circuit including,

a second transistor coupled to the first node and adapted to conduct a second current from the first node in response to the first phase of the input signal and adapted to provide a first phase of an output signal at a second node, wherein a magnitude of the first phase of the output signal is proportional to a magnitude of the second current; and

an impedance circuit coupled to the first node, the impedance circuit adapted to decrease a magnitude of the first current in response to an increased frequency of the input signal and further adapted to increase the magnitude of the second current in response to the increased frequency of the input signal.

23. (New) The amplifier of claim 22, wherein the impedance circuit comprises:

a first inductor having a first conductor and a second conductor, wherein the first conductor is coupled to a power supply node;

a first resistor having a first conductor and a second conductor, wherein the first conductor is coupled to the second conductor of the first inductor; and

a first capacitor having a first conductor coupled to the second conductor of the first resistor at the first node.

24. (New) The amplifier of claim 23 wherein the boost circuit further includes:

a third transistor coupled to a third node and adapted to conduct the first current from the third node in response to a second phase of the input signal.

25. (New) The amplifier of claim 24 wherein the inductive amplifier circuit further includes:

a fourth transistor coupled to the third node and adapted to conduct the second current from the third node in response to the second phase of the input signal and adapted to provide a second phase of the output signal at a fourth node, wherein a magnitude of the second phase of the output signal is proportional to the magnitude of the second current.

26. (New) The amplifier of claim 25, wherein the impedance circuit further comprises:

a second inductor having a first conductor and a second conductor, wherein the first conductor is coupled to the power supply node;

a second resistor having a first conductor and a second conductor, wherein the first conductor is coupled to the second conductor of the second inductor; and

a second capacitor having a first conductor coupled to the second conductor of the second resistor at the third node, the second capacitor having a second conductor coupled to a second conductor of the first capacitor.